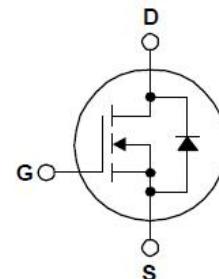
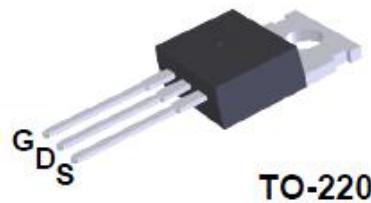


150V N-Channel MOSFET

Features

- $V_{DSS}=150V$ / $I_D=45A$
- $R_{DS(On)}=27m\Omega$ (Typ.)@ $V_{GS}=10V$
- Low On-Resistance
- Low Input Capacitance
- Low Miller Charge
- Low Input / Output Leakage

PIN DESCRIPTION



Applications

- Motor / Body Load Control
- Automotive Systems
- Solenoid and Motor Control
- DC-DC converters and Off-line UPS

Part Number	Package	Marking	ROHS Status	Packing
SI150N03B	TO-220	SI150N03B	Halogen-Free	Tube&Box

Absolute Maximum Ratings ($T_A=25^\circ C$ unless otherwise noted)

Symbol	Parameter	Value	Unit
V_{DSS}	Drain-Source Voltage	150	V
V_{GSS}	Gate-Source Voltage	± 30	V
I_D	Drain Current-Continuous	$T_C=25^\circ C$	A
		$T_C=70^\circ C$	A
I_{DM}	Drain Current-Pulsed ^{NOTE 1}	180	A
E_{AS}	Avalanche Energy, $L=3mH$, $V_G=10V$, Rated $V_{DS}=150V$	180	mJ
I_{AS}	Avalanche Current, $L=3mH$, $V_G=10V$, Rated $V_{DS}=150V$	10	A
P_D	Maximum Power Dissipation	$T_C=25^\circ C$	W
		$T_A=25^\circ C$	W
T_J	Operating Junction Temperature	-55 to 150	°C
T_{STG}	Storage Temperature Range	-55 to 150	°C

Thermal Resistance Ratings

Symbol	Parameter	Conditions	Max.	Unit
$R_{\theta JA}$	Maximum Junction-to-Ambient ^{NOTE2}	Steady State	62	°C/W
$R_{\theta JC}$	Maximum Junction-to-Case	Steady State	1.2	°C/W

Electrical Characteristics ($T_J=25^\circ\text{C}$ unless otherwise noted)

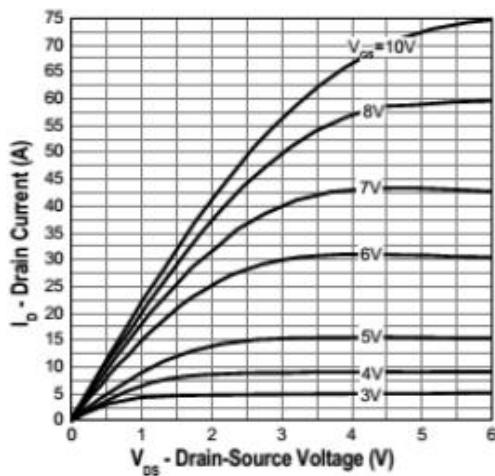
Symbol	Parameter	Test Conditions	Min	TYP	Max	Unit
Static Characteristics						
BV_{DSS}	Drain-source breakdown voltage	$V_{\text{GS}}=0\text{V}, I_{\text{DS}}=250\mu\text{A}$	150	-	-	V
$V_{\text{GS}(\text{TH})}$	Gate threshold voltage	$V_{\text{DS}}=V_{\text{GS}}, I_{\text{DS}}=250\mu\text{A}$	2	-	4	V
I_{DSS}	Zero gate voltage drain current	$V_{\text{DS}}=120\text{V}, V_{\text{GS}}=0\text{V}$	-	-	1	μA
I_{GSS}	Gate-source leakage current	$V_{\text{GS}}=\pm 30\text{V}, V_{\text{DS}}=0\text{V}$	-	-	± 100	nA
$R_{\text{DS}(\text{on})}$	Drain-source on-state resistance	$V_{\text{GS}}=10\text{V}, I_{\text{DS}}=40\text{A}$	-	27	34	$\text{m}\Omega$
Dynamic Characteristic						
C_{iss}	Input Capacitance	$V_{\text{GS}}=0\text{V}, V_{\text{DS}}=30\text{V}, f=1\text{MHz}$	-	1933	-	pF
C_{oss}	Output Capacitance		-	147	-	
C_{rss}	Reverse Transfer Capacitance		-	49	-	
Switching Characteristics						
Q_g	Total Gate Charge at 4.5V	$V_{\text{GS}}=10\text{V}, V_{\text{DS}}=75\text{V}, I_{\text{DS}}=15\text{A}$	-	55	-	nc
Q_{gs}	Gate-Source charge		-	18	-	
Q_{gd}	Gate-Drain charge		-	17	-	
$T_{\text{d}(\text{on})}$	Turn-on delay time	$V_{\text{GS}}=10\text{V}, V_{\text{DS}}=75\text{V}, R_{\text{GEM}}=3\Omega, I_{\text{D}}=15\text{A}$	-	22	-	ns
t_r	Rise time		-	10	-	ns
$T_{\text{d}(\text{off})}$	Turn-off delay time		-	12	-	us
t_f	Fall time		-	35	-	us
Diode Characteristic						
V_{SD}	Drain-Source Diode Forward Voltage	$V_{\text{GS}}=0\text{V}, I_{\text{S}}=15\text{A}$	-	-	1.3	V
t_{rr}	Body Diode Reverse Recovery Time	$I_{\text{f}}=15\text{A}, T_J=25^\circ\text{C}$ $dI/dt=500\text{A}/\mu\text{s}$	-	25	-	nS
Q_{rr}	Body Diode Reverse Recovery Charge		-	32	-	nC

Notes:

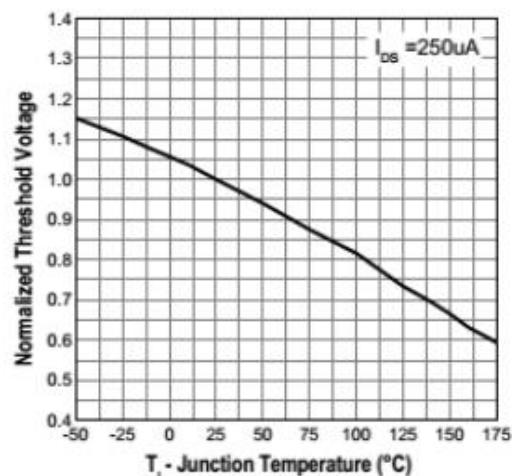
1. Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$.
2. $R_{\Theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\Theta JC}$ is guaranteed by design while $R_{\Theta CA}$ is determined by the user's board design. $R_{\Theta JA}$ shown below for single device operation on FR-4 instill air

Typical Performance Characteristics

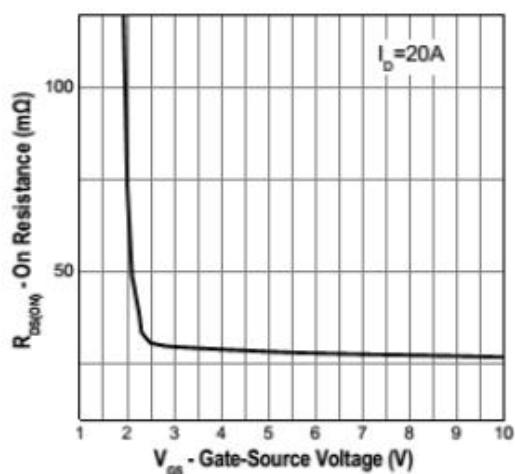
Output Characteristics



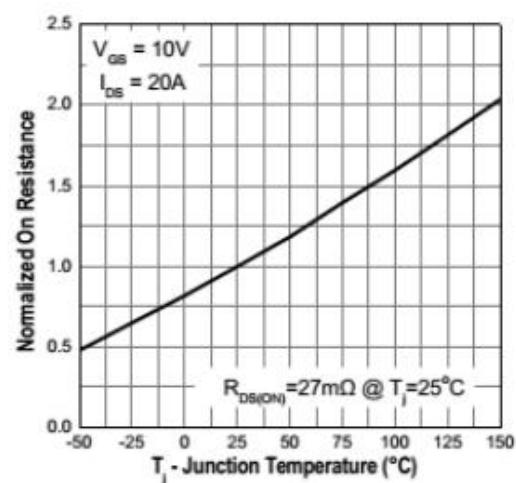
Gate Threshold Voltage



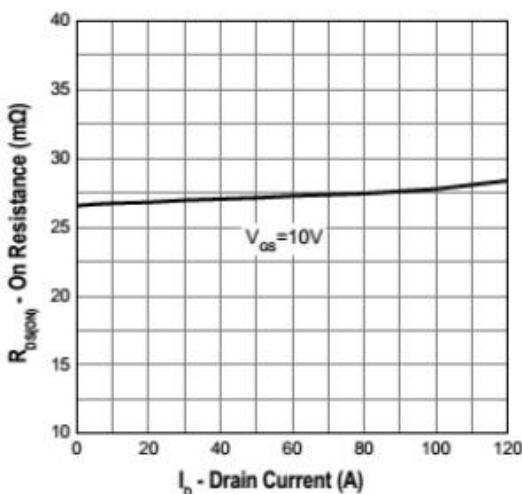
Gate-Source On Resistance



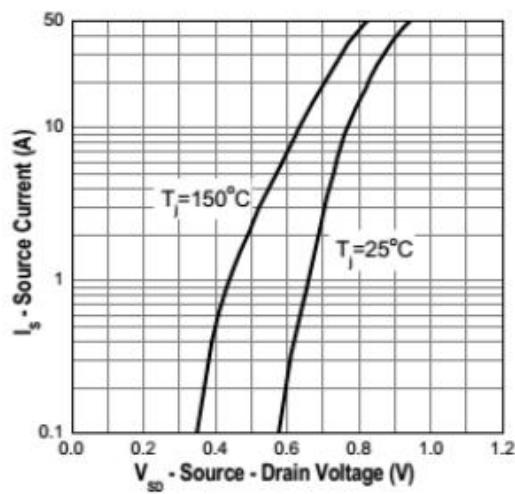
Drain-Source On Resistance



Drain-Source On Resistance

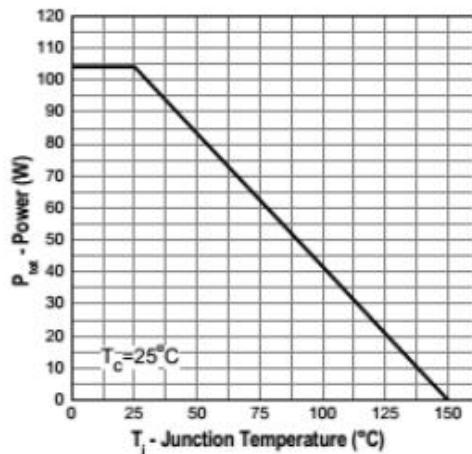


Source-Drain Diode Forward

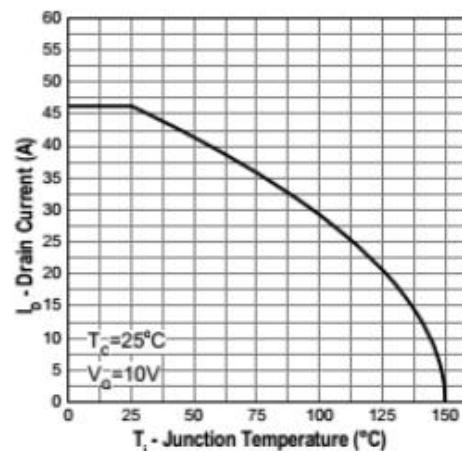


Typical Performance Characteristics (Cont.)

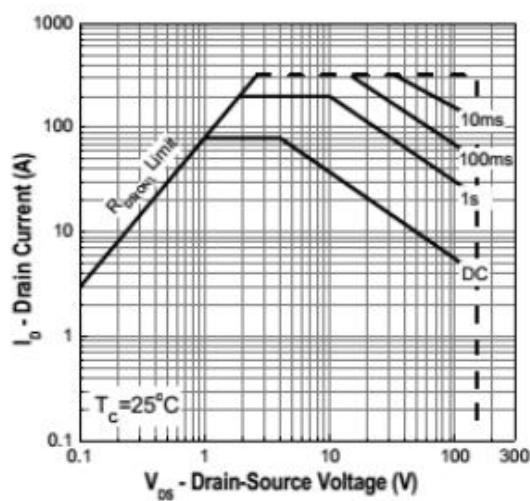
Power Dissipation



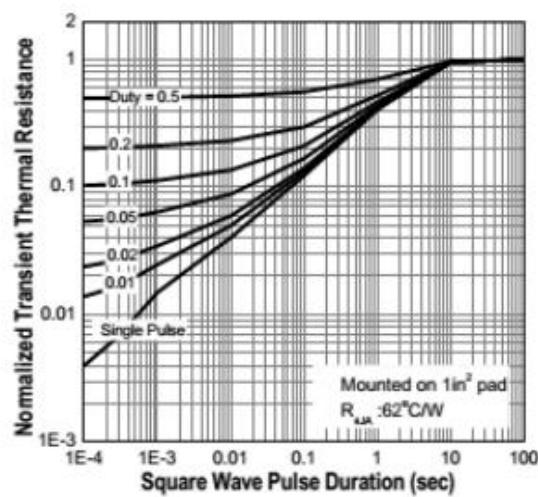
Drain Current



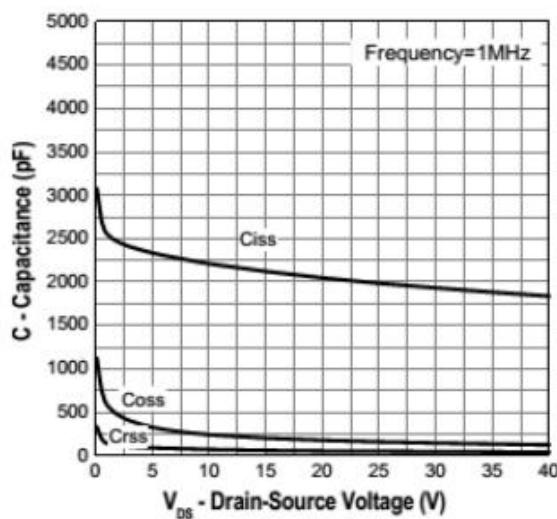
Safe Operation Area



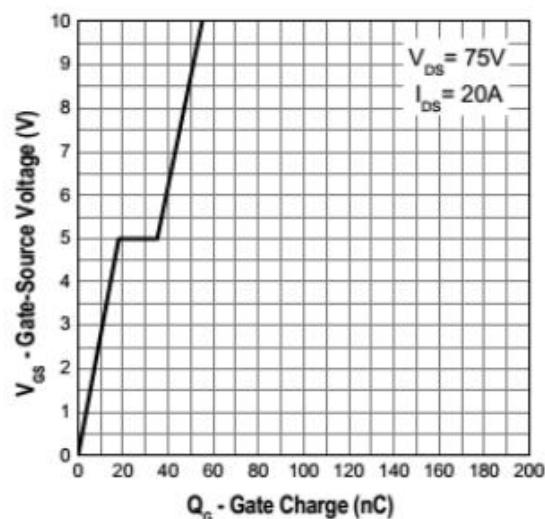
Transient Thermal Impedance



Capacitance



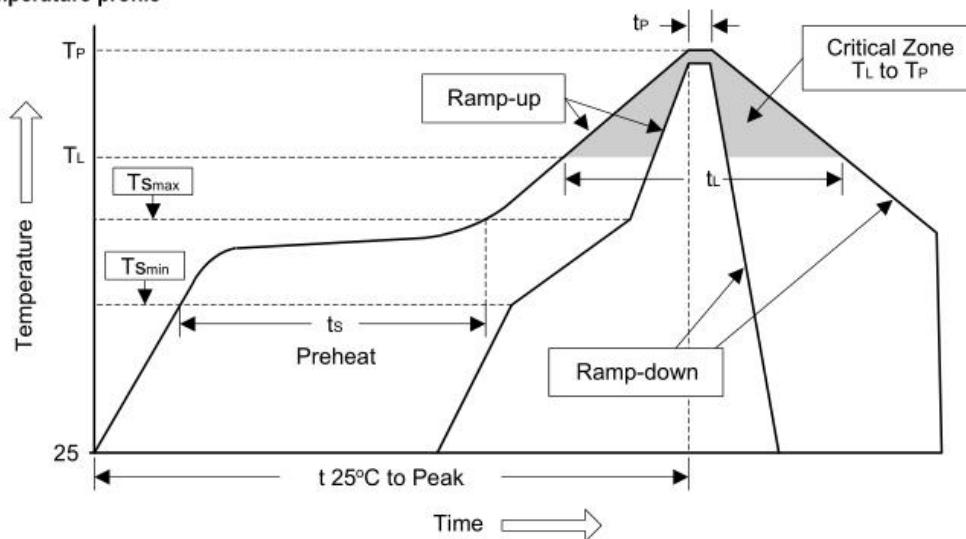
Gate Charge



Soldering Methods for Products

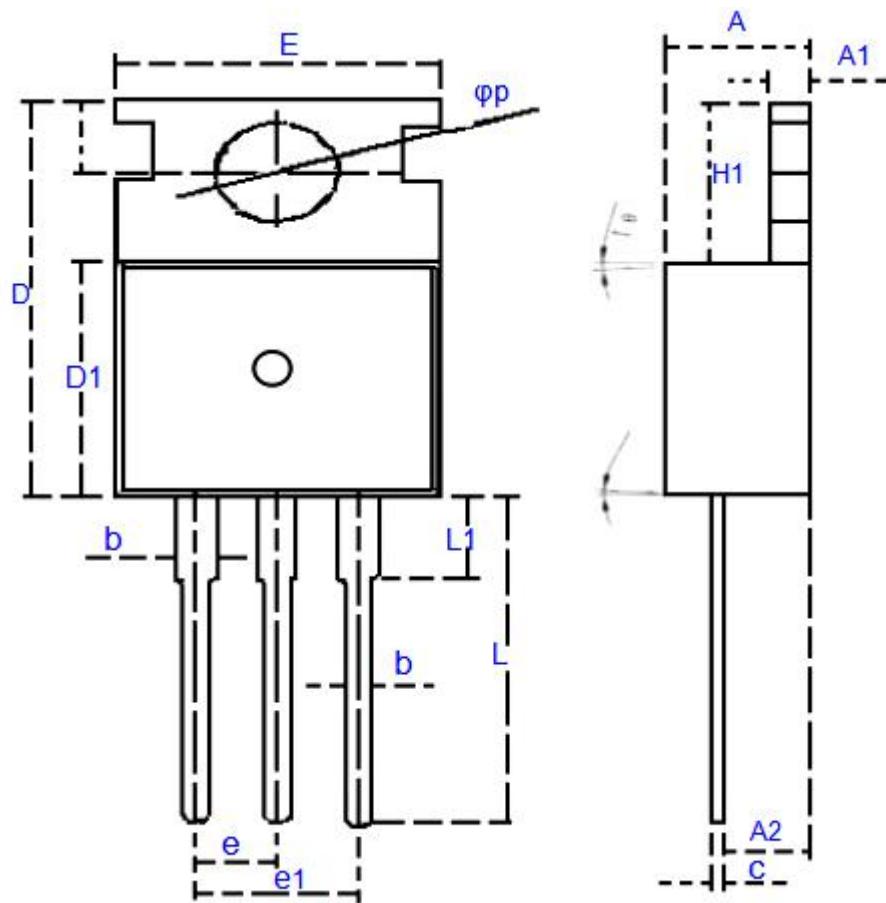
Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average ramp-up rate(TL to TP)	<3°C/sec	<3°C/sec
Preheat	-	-
-Temperature Min(Ts min)	100°C	150°C
-Temperature Max(Ts max)	150°C	200°C
-Time(min to max)(ts)	60 to 120 sec	60 to 180 sec
Ts max to TL	<3°C/sec	<3°C/sec
- ramp-up rate		
Time maintained above:		
-Temperature(TL)	183°C	217°C
-Time(TL)	60 to 150 sec	60 to 150 sec
Peak Temperature(TP)	240°C+0/-5°C	260°C+0/-5°C
Time within 5°C of actual Peak Temperature	10 to 30 sec	20 to 40 sec
Ramp-down Rate	<6°C/sec	<6°C/sec
Time 25 °C to Peak Temperature	<6 minutes	<8 minutes

Figure 1: Temperature profile



- Note :**
- 1.Storage environment: Temperature=10°C to 35@Humidity=45%±15%
 - 2.Reflow soldering of surface-mount devices
 - 3.Flow(wave) soldering(solder dipping)

Products	Peak Temperature	Dipping Time
Pb devices	245°C±5°C	5sec±1sec
Pb-free devices	260°C+0/-5°C	5sec±1sec

■ Package Outline


Millimeters					
Symbol	Min	Max	Symbol	Min	Max
A	4.2	4.8	E	9.6	10.5
A1	1.28	1.34	e	2.54 Typ.	
A2	2.2	2.6	e1	5.08	5.18
b	0.69	0.91	H1	6.1	7.0
b1	1.17	1.37	L	12.9	13.5
c	0.42	0.51	L1	2.9	3.7
D	15.1	16.3	ΦP	3.4	3.8
D1	9.0	9.5	θ1 (°)	1	5

■ Important Notice

Si-Trend reserves the right to change all product ,product specifications and data without prior notice ; Our customer Please confirm to place an order confirmation before make the integrity of information complete and up-to-date .

Any semiconductor under specific conditions are possible to certain failure or malfunction rate : Customers are responsible in the use of Si-Trend products to system design and manufacturing in compliance with safety standards and adopting safety measures ,To avoid the potential risk of failure may cause the personal safety and property loss .

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■ Modify record

Date	Version	Description	Pagination
20160914	A.0	original	7
20190820	A.1	/	7