

30V P-Channel Fast Switching MOSFET

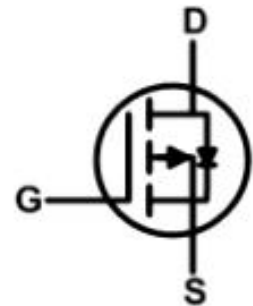
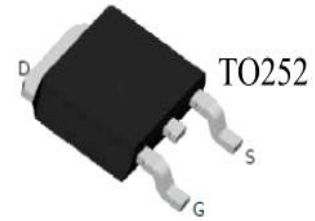
Features

- $V_{DSS} = -30V$ $I_D = -35A$
- $R_{DS(ON)} = 20m\Omega(\text{max.}) @ V_{GS} = -10V$
- $R_{DS(ON)} = 32m\Omega(\text{max.}) @ V_{GS} = -4.5V$
- Low On-Resistance
- Excellent CdV/dt effect decline
- Super Low Gate Charge
- 100% EAS Guaranteed
- Green Device Available
- Advanced high cell density Trench technology

Applications

- The SI3103D is the high cell density trenched P-ch MOSFETs, which provide excellent $R_{DS(ON)}$ and Q-gate charge for most of the synchronous buck converter applications.
- The SI3103D meet the ROHS and Green Product requirement, 100% EAS guaranteed with full function reliability approved.

PIN DESCRIPTION



Part Number	Package	Marking	ROHS Status	Packing
SI3103D	TO-252	D3103	Halogen-Free	Tape&Reel

Absolute Maximum Ratings ($T_A = 25^\circ C$ unless otherwise noted)

Symbol	Parameter	Ratings	Unit	
V_{DS}	Drain-Source Voltage	-30	V	
V_{GS}	Gate-Source Voltage	± 20	V	
I_D	Continuous Drain Current, $V_{GS} = -10V$	$T_c = 25^\circ C$	-35	A
		$T_c = 100^\circ C$	-22	A
I_{DM}	Pulsed Drain Current	-70	A	
I_{AS}	Avalanche Current	-38	A	
E_{AS}	Single Pulse Avalanche Energy	37	mJ	
T_J, T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150	$^\circ C$	
P_D	Total Power Dissipation	$T_c = 25^\circ C$	34.7	W

THERMAL RESISTANCE RATINGS

Symbol	Parameter	Typical	Max	Unit
$R_{\theta JA}$	Thermal resistance Junction-to-Ambient	-	62	$^\circ C/W$
$R_{\theta JC}$	Thermal resistance Junction-to-Case	-	3.6	

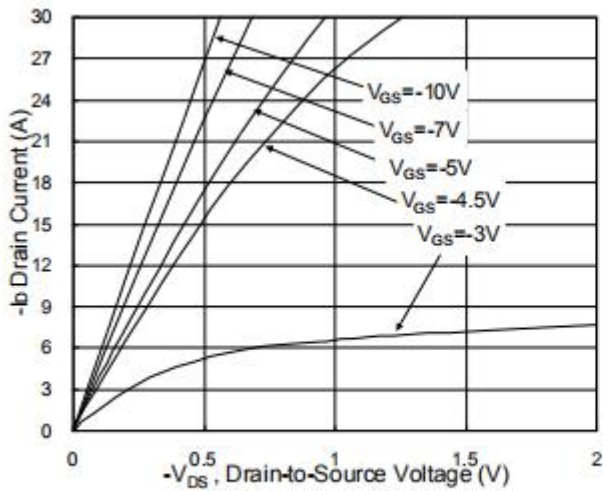
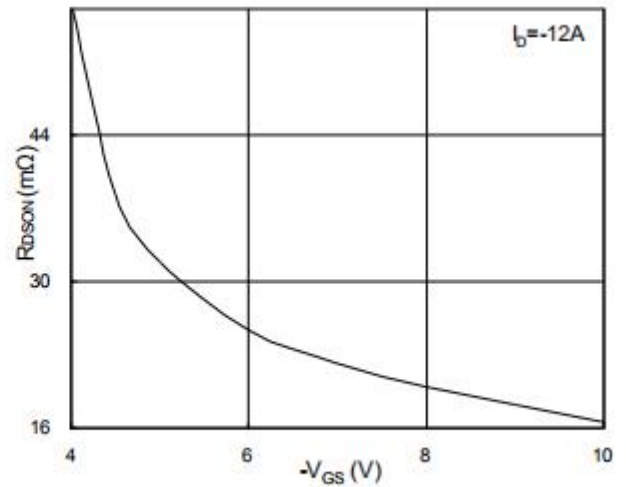
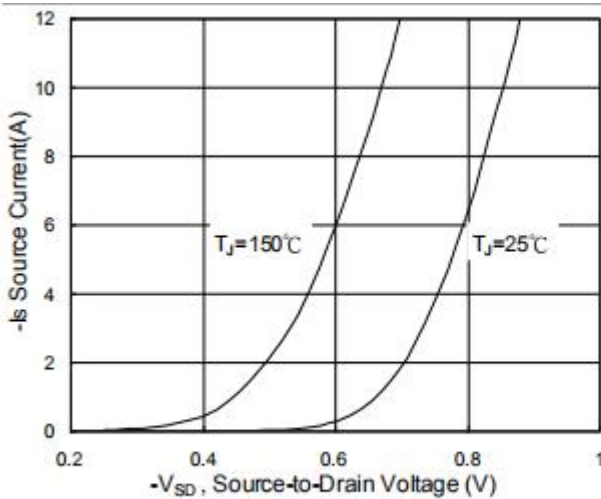
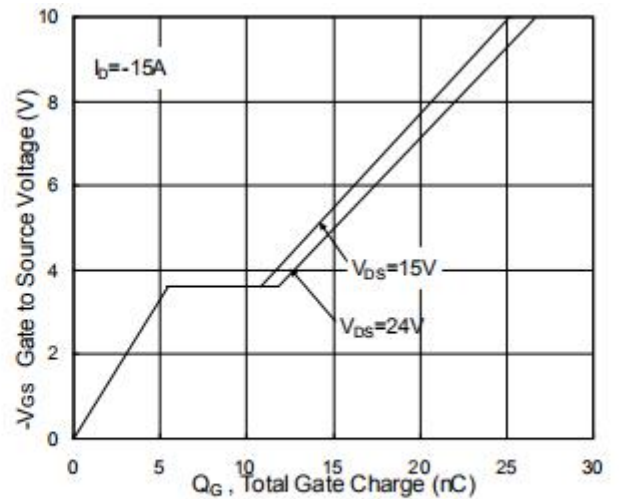
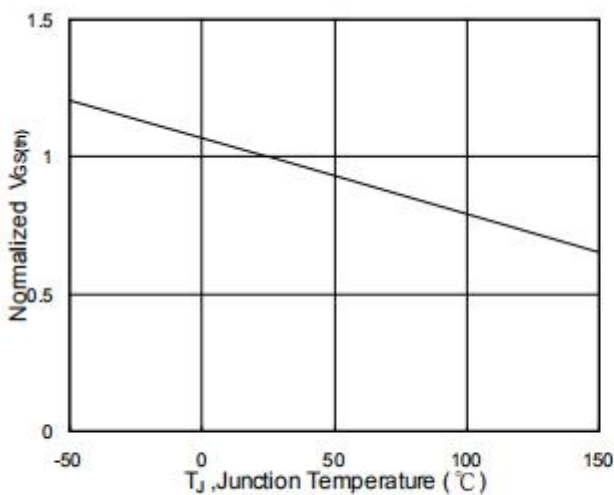
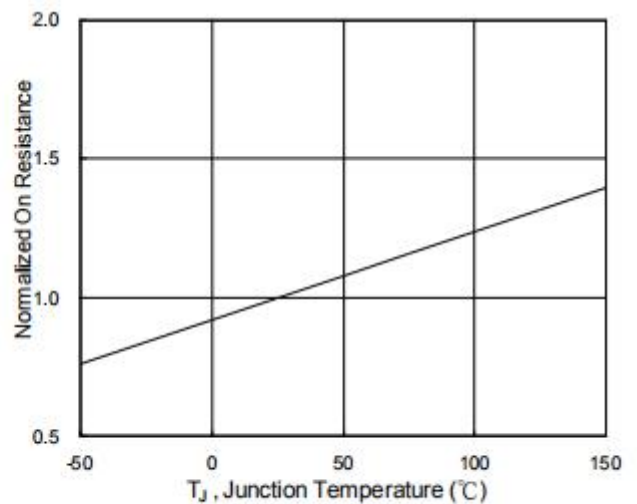
Electrical Characteristics (T_J=25°C unless otherwise Ratings)

Symbol	Parameter	Test Conditions	Min.	TYP.	Max.	Unit
Static Characteristics						
B _V DSS	Drain-source breakdown voltage	V _{GS} =0V, I _{DS} = -250uA	-30	-	-	V
V _{GS(th)}	Gate threshold voltage	V _{DS} =V _{GS} , I _{DS} =-250uA	-1.0	-	-2.5	V
I _{DSS}	Drain-Source Leakage Current	V _{DS} =-32V, V _{GS} =0V, T _J =2°C	-	-	-1	uA
		V _{DS} =-32V, V _{GS} =0V, T _J =5°C	-	-	-5	uA
I _{GSS}	Gate-source leakage current	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
R _{DS(on)}	Drain-source on-state resistance	V _{GS} =-10V, I _D =-15A	-	-	20	mΩ
		V _{GS} = -4.5V, I _D =-10A	-	-	32	mΩ
G _{fs}	Forward Transconductance	V _{DS} =-5V , I _D =-10A	-	5	-	S
R _g	Gate Resistance	V _{DS} =0V, V _{GS} =0V , f=1MHz	-	13	-	Ω
Dynamic Characteristic						
Q _g	Total Gate Charge	V _{GS} =-4.5V, V _{DS} =-15V I _D =-15A	-	12.5	-	nC
Q _{gs}	Gate-Source Charge		-	5.4	-	nC
Q _{gd}	Gate-Drain Charge		-	5	-	nC
T _{d(on)}	Turn-on delay time	I _D =-15A, V _{GS} =-10V V _{DD} =-15V, R _G =3.3Ω	-	4.4	-	nS
T _r	Rise time		-	11.2	-	nS
T _{d(off)}	Turn-off delay time		-	34	-	nS
T _f	Fall time		-	18	-	nS
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =-15V, f=1.0MHz	-	1345	-	pF
C _{oss}	Output Capacitance		-	194	-	pF
C _{rss}	Reverse Transfer Capacitance		-	158	-	pF
Source-Drain Diode						
V _{SD}	Diode Forward Voltage	V _{GS} =0V, I _S =-1A	-	-	-1.2	V
I _{SM}	Pulsed Source Current	V _G =V _D =0V Force Current	-	-	-70	A
I _S	Continuous Source Current		-	-	-35	A
t _{rr}	Reverse Recovery Time	I _F =15A , T _J =25°C dI/dt=100A/μs ,	-	12.4	-	nS
Q _{rr}	Reverse Recovery Charge		-	5	-	nC

Notes:

- The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- The data tested by pulsed , pulse width ≅ 300us , duty cycle ≅ 2%
- The E_{AS} data shows Max.rating .The test condition is V_{DD}=-25V, V_{GS}=-10V, L=0.1mH, I_{AS}=-38A
- The power dissipation is limited by 150 °C junction temperature
- The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

Typical Performance Characteristics


Fig.1 Typical Output Characteristics

Fig.2 On-Resistance v.s Gate-Source

Fig.3 Forward Characteristics of Reverse

Fig.4 Gate-Charge Characteristics

Fig.5 Normalized $V_{GS(th)}$ v.s T_J

Fig.6 Normalized $R_{DS(on)}$ v.s T_J

Typical Performance Characteristics (Cont.)

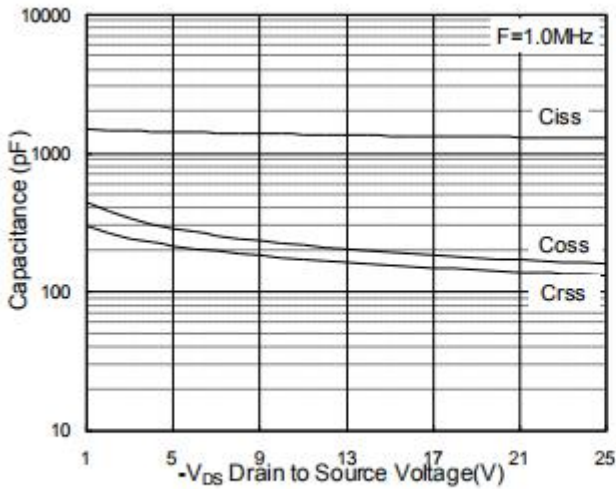


Fig.7 Capacitance

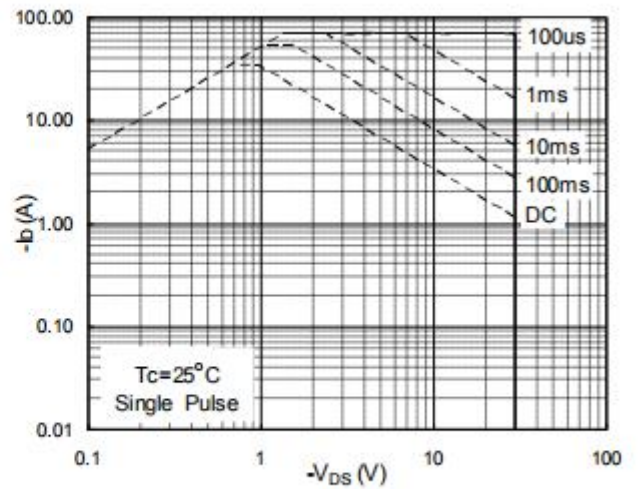


Fig.8 Safe Operating Area

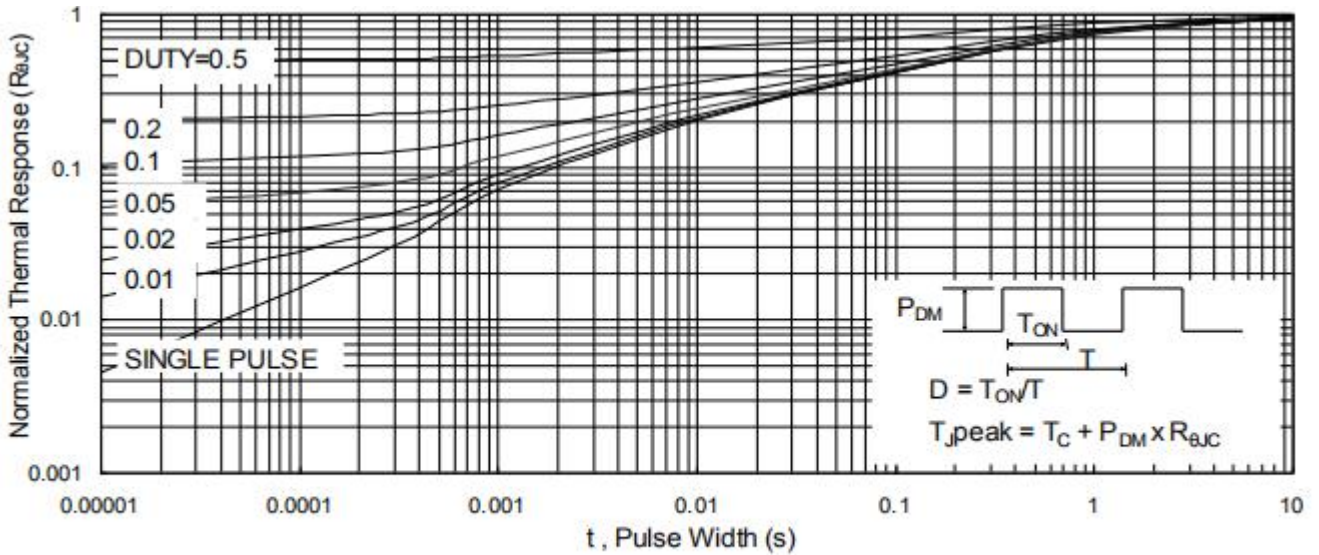


Fig.9 Normalized Maximum Transient Thermal Impedance

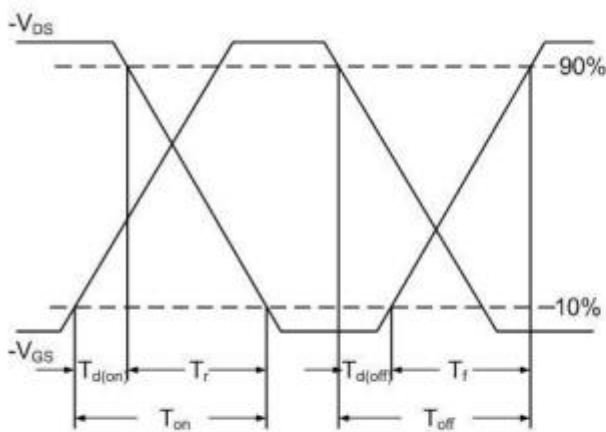


Fig.10 Switching Time Waveform

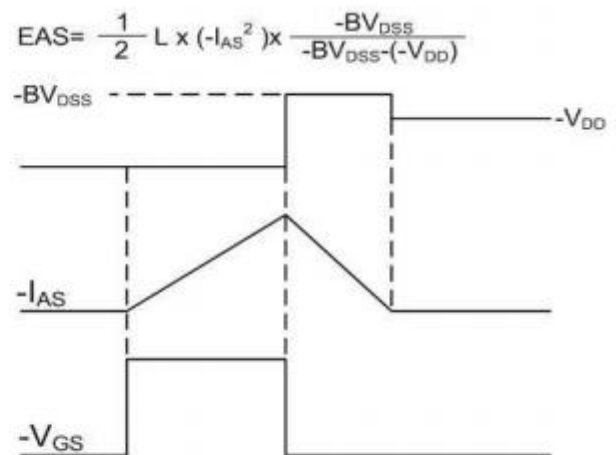
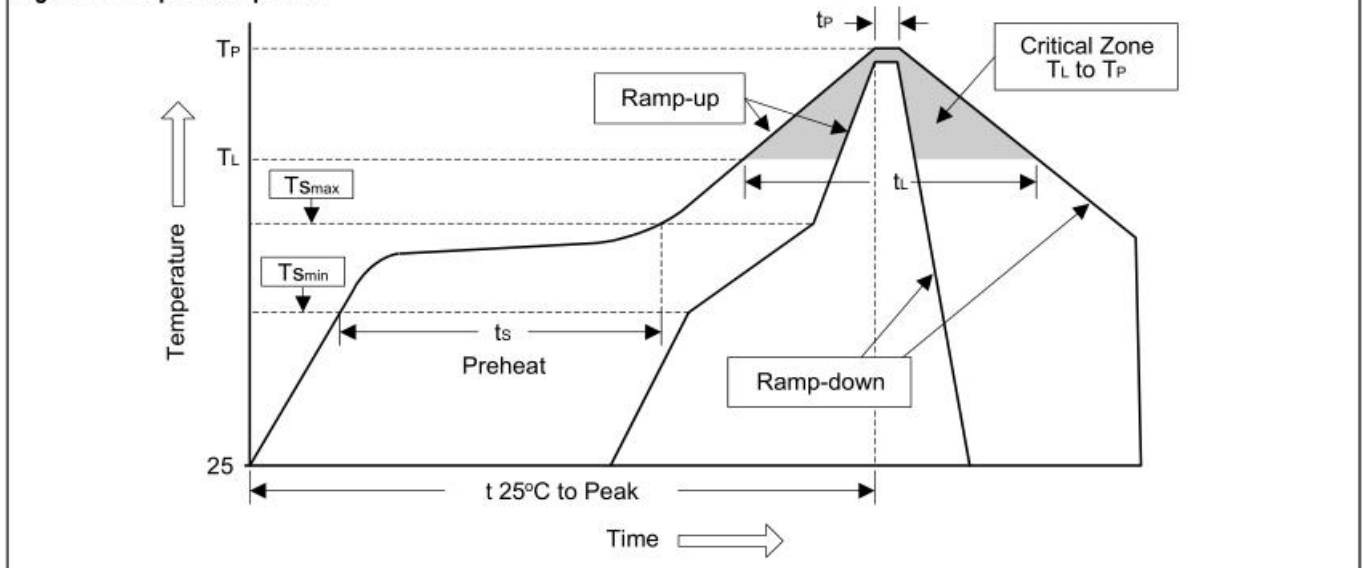


Fig.11 Unclamped Inductive Switching Waveform

Soldering Methods for Products

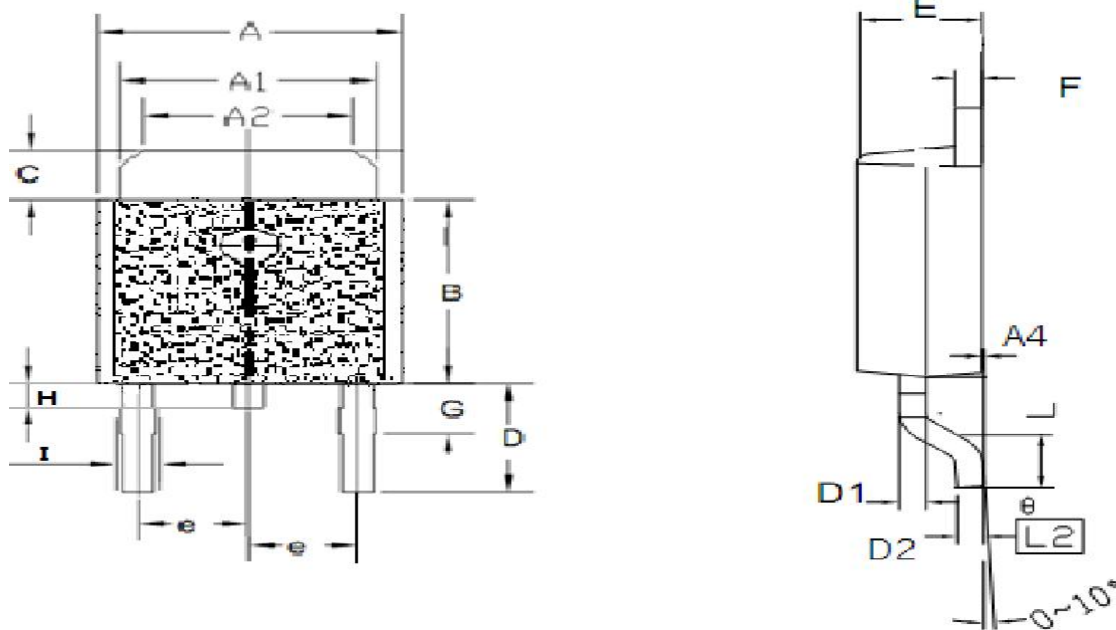
Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average ramp-up rate(TL to TP)	<3°C/sec	<3°C/sec
Preheat	-	-
-Temperature Min(Ts min)	100°C	150°C
-Temperature Max(Ts max)	150°C	200°C
-Time(min to max)(ts)	60 to 120 sec	60 to 180 sec
Ts max to TL		
- ramp-up rate	<3°C/sec	<3°C/sec
Time maintained above:		
-Temperature(TL)	183°C	217°C
-Time(TL)	60 to 150 sec	60 to 150 sec
Peak Temperature(TP)	240°C+0/-5°C	250°C+0/-5°C
Time within 5°C of actual Peak Temperature	10 to 30 sec	20 to 40 sec
Ramp-down Rate	<6°C/sec	<6°C/sec
Time 25 °C to Peak Temperature	<6 minutes	<8 minutes

Figure 1: Temperature profile



- Note :**
- 1.Storage environment: Temperature=10°C to 35@Humidity=45%±15%
 - 2.Reflow soldering of surface-mount devices
 - 3.Flow(wave) soldering(solder dipping)

Products	Peak Temperature	Dipping Time
Pb devices	245°C±5°C	5sec±1sec
Pb-free devices	250°C+0/-5°C	5sec±1sec

Package Outline


unit: mm					
Symbol	Min	Max	Symbol	Min	Max
A	6.40	6.60	D	2.90	3.10
A1	5.20	5.40	D1	0.45	0.55
A2	4.40	4.60	D2	0.45	0.55
A3	4.40	4.60	e	2.3BSC	
A4	0.00	0.15	E	2.20	2.40
A5	4.65	4.95	F	0.49	0.59
B	6.00	6.20	G	1.7BSC	
B1	1.57	1.77	L	1.40	1.60
C	0.90	0.96	θ (度)	0.00	10.00
I	0.80	0.85	H	0.49	0.52

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